FEATURES
Complete Sampling 16-Bit ADC With Reference and Clock
50 kHz Throughput
±1/2 LSB Nonlinearity
Low Noise SHA: 300 μV p-p
32-Pin Hermetic DIP
Parallel and Serial Outputs
Low Power: 900 mW

APPLICATIONS
Medical and Analytical Instrumentation
Signal Processing
Data Acquisition Systems
Professional Audio
Automatic Test Equipment (ATE)
Telecommunications

PRODUCT DESCRIPTION
The AD1380 is a complete, low cost 16-bit analog-to-digital converter, including internal reference, clock and sample/hold amplifier. Internal thin-film-on-silicon scaling resistors allow analog input ranges of ±2.5 V, ±5 V, ±10 V, 0 V to +5 V and 0 V to +10 V.

Important performance characteristics of the AD1380 include maximum linearity error of ±0.003% of FSR (AD1380KD) and maximum 16-bit conversion time of 14 μs. Transfer characteristics of the AD1380 (gain, offset and linearity) are specified for the combined ADC/SHA, so total performance is guaranteed as a system. The AD1380 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL or 5 V CMOS compatible.
## AD1380—SPECIFICATIONS

(typical @ $T_A = +25^\circ C$, $V_S = +15$ V, $+5$ V combined sample-and-hold A/D converter unless otherwise noted)

<table>
<thead>
<tr>
<th>Model</th>
<th>AD1380JD</th>
<th>AD1380KD</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td>16</td>
<td>*</td>
<td>Bits</td>
</tr>
<tr>
<td>ANALOG INPUTS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bipolar</td>
<td>$\pm 2.5, \pm 5, \pm 10$</td>
<td>*</td>
<td>Volts</td>
</tr>
<tr>
<td>Unipolar</td>
<td>0 to $+5$, 0 to $+10$</td>
<td>*</td>
<td>Volts</td>
</tr>
<tr>
<td>DIGITAL INPUTS$^1$</td>
<td>Convert Command</td>
<td>TTL Compatible</td>
<td>*</td>
</tr>
<tr>
<td>Logic Loading</td>
<td>1</td>
<td>*</td>
<td>LSTTL Load</td>
</tr>
</tbody>
</table>

### TRANSFER CHARACTERISTICS$^2$

(COMBINED ADC/SHA)

- **Gain Error**: $\pm 0.1\%$, $\pm 0.05$ typ$^3$
- **Unipolar Offset Error**: $\pm 0.05\%$, $\pm 0.02$ typ$^3$
- **Bipolar Zero Error**: $\pm 0.05\%$, $\pm 0.02$ typ$^3$
- **Linearity Error**: $\pm 0.006\%$ FSR$^4$
- **Differential Linearity Error**: $\pm 0.003\%$ FSR$^4$
- **Noise (10 V Unipolar)**: 85 $\mu$V rms
- **(20 V Bipolar)**: 115 $\mu$V rms

### THROUGHPUT

- **Conversion Time**: 14 max $\mu$s
- **Acquisition Time (20 V Step)**: 6 max $\mu$s

### SAMPLE & HOLD

- **Input Resistance**: 4 k$\Omega$
- **Small Signal Bandwidth**: 900 kHz
- **Aperture Time**: 50 ns
- **Aperture Jitter**: 100 ps
- **Drop Rate**: 50 $\mu$m/s
- **$T_{MIN}$ to $T_{MAX}$**: 1
- **Feedthrough**: $-80$ dB

### DRIFT (ADC & SHA)$^5$

- **Gain**: $\pm 20$ max $\%$ FSR
- **Unipolar Offset**: $\pm 5$ max ($\pm 2$ typ)
- **Bipolar Zero**: $\pm 5$ max ($\pm 2$ typ)
- **No Missing Codes (Guaranteed)**: 0 to $+70$ (13 Bits) 0 to $+70$ (14 Bits)

### DIGITAL OUTPUTS

- **TTL Compatible: 5**
- **Clock Frequency**: 1.1 MHz

### POWER SUPPLY REQUIREMENTS

- **Analog Supplies**: $\pm 15 \pm 0.5$ V
- **Digital Supply**: $+5 \pm 0.25$ V
- **$+15$ V Supply Current**: 25 mA
- **$-15$ V Supply Current**: 30 mA
- **$+5$ V Supply Current**: 15 mA
- **Power Dissipation**: 900 mW

### TEMPERATURE RANGE

- **Specified**: 0 to $+70$ $^\circ$C
- **Operating**: $-25$ to $+85$ $^\circ$C

### NOTES

1. Logic “0” = 0.8 V, max. Logical “1” = 2.0 V, min for inputs. For digital outputs Logic “0” = 0.4 V max. Logical “1” = 2.4 V min.
2. Tested on $+10$ V and 0 V to $+10$ V ranges.
3. Adjustable to zero.
4. Full-scale range.
5. Guaranteed but not 100% production tested.

*Specifications same as AD1380JD.*

Specifications subject to change without notice.
ABSOLUTE MAXIMUM RATINGS
Supply Voltage ........................................ +18 V
Logic Supply Voltage ................................. +7 V
Analog Ground to Digital Ground .................. +0.3 V
Analog Inputs (Pins 6, 7, 31) ........................ ±Vg
Digital Input ........................................... -0.3 V to VDD +0.3 V
Output Short Circuit Duration to Ground
Sample/Hold .............................. 1 sec for Any One Output
Junction Temperature ................................. +175°C
Storage Temperature ................................. -65°C to +150°C
Lead Temperature (Soldering, 10 sec) .............. +300°C

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Max Linearity Error</th>
<th>Temperature Range</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD1380JD</td>
<td>0.006% FSR</td>
<td>0°C to +70°C</td>
<td>Ceramic (DH-32E)</td>
</tr>
<tr>
<td>AD1380KD</td>
<td>0.003% FSR</td>
<td>0°C to +70°C</td>
<td>Ceramic (DH-32E)</td>
</tr>
</tbody>
</table>

THEORY OF OPERATION
A 16-bit A/D converter partitions the range of analog inputs into $2^{16}$ discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2 LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 2 and 3. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential non-linearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 1).

Monotonic behavior requires that the differential linearity error be less than 1 LSB; however, a monotonic converter can have missing codes. The AD1380 is specified as having no missing codes over temperature ranges as specified on the data page.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1380 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full-scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$\text{RSS} = \sqrt{\epsilon_G^2 + \epsilon_0^2 + \epsilon_L^2}$$

$\epsilon_G$ = Gain Drift Error (ppm/°C)
$\epsilon_0$ = Offset Drift Error (ppm of FSR/°C)
$\epsilon_L$ = Linearity Error (ppm of FSR/°C)

![Figure 1. Transfer Characteristics for an Ideal Bipolar A/D](image)

DESCRIPTION OF OPERATION
On receipt of a CONVERT START command, the AD1380 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive approximation register (SAR) has its 16-bit outputs connected to both the device bit output pins and the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

REV. B

-3-
AD1380

GAIN ADJUSTMENT
The gain adjust circuit consists of a 100 ppm/°C potentiometer connected across ±V with its slider connected through a 300 kΩ resistor to the gain adjust Pin 3 as shown in Figure 2. If no external trim adjustment is desired, Pin 5 (OFFSET ADJ) and Pin 3 (GAIN ADJ) may be left open.

OFFSET ADJUSTMENT
The zero adjust circuit consists of a 100 ppm/°C potentiometer connected across ±V with its slider connected through a 1.8 MΩ resistor to Comparator Input Pin 5 for all ranges. As shown in Figure 3, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200 ppm/°C tempco contributes a worst-case offset tempco of 32 LSB14 x 61 ppm/LSB14 x 1200 ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB14, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

Figure 3. Offset Adjustment Circuit (±0.3% FSR)
An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 4.

Figure 4. Low Tempco Zero Adjustment Circuit
In either adjust circuit, the fixed resistor connected to Pin 5 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 5 is quite sensitive to external noise pickup and should be guarded by analog common.

TIMING
The timing diagram is shown in Figure 5. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock permitting it to run through 17 cycles. All the
SAR parallel bits, STATUS flip-flops and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t0, B1 is reset and B2 - B16 are set unconditionally. At t1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t16. The STATUS flag is reset, indicating that the conversion is complete and the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic “0” state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

DIGITAL OUTPUT DATA
Both parallel and serial data from TTL storage registers is in negative true form (Logic “1” = 0 V and Logic “0” = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic “0,” permitting parallel data transfer to be clocked on the “1” to “0” transition of the STATUS flag (see Figure 6).

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 7. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

INPUT SCALING
The AD1380 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table I. See Figure 8 for circuit details.

![Figure 7. Clock High to Serial Out Valid](image)

**Figure 7. Clock High to Serial Out Valid**

**Table I. AD1380 Input Scaling Connections**

<table>
<thead>
<tr>
<th>Input Signal Range</th>
<th>Output Code</th>
<th>Connect Pin 4 to Pin</th>
<th>Connect Pin 7 to</th>
<th>Connect Input Signal to</th>
</tr>
</thead>
<tbody>
<tr>
<td>±10 V</td>
<td>COB</td>
<td>5</td>
<td>Input Signal 7</td>
<td>7</td>
</tr>
<tr>
<td>±5 V</td>
<td>COB</td>
<td>5</td>
<td>Open</td>
<td>6</td>
</tr>
<tr>
<td>±2.5 V</td>
<td>COB</td>
<td>5</td>
<td>Pin 5</td>
<td>6</td>
</tr>
<tr>
<td>0 V to +5 V</td>
<td>CSB</td>
<td>NC</td>
<td>Pin 5</td>
<td>6</td>
</tr>
<tr>
<td>0 V to +10 V</td>
<td>CSB</td>
<td>NC</td>
<td>Open</td>
<td>6</td>
</tr>
</tbody>
</table>

**NOTE**
Pin 5 is extremely sensitive to noise and should be guarded by analog common.
Table II. Transition Values vs. Calibration Codes

<table>
<thead>
<tr>
<th>Code Under Test</th>
<th>Range</th>
<th>±10 V</th>
<th>±5 V</th>
<th>±2.5 V</th>
<th>0 V to +10 V</th>
<th>0 V to +5 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>000...000*</td>
<td>+ Full Scale</td>
<td>+10 V</td>
<td>+5 V</td>
<td>+2.5 V</td>
<td>+10 V</td>
<td>+5 V</td>
</tr>
<tr>
<td>011...111</td>
<td>Mid Scale</td>
<td>0–1/2 LSB</td>
<td>0–1/2 LSB</td>
<td>0–1/2 LSB</td>
<td>5 V–1/2 LSB</td>
<td>+2.5 V–1/2 LSB</td>
</tr>
<tr>
<td>111...110</td>
<td>–Full Scale</td>
<td>−10 V</td>
<td>−5 V</td>
<td>−2.5 V</td>
<td>0 V</td>
<td>0 V</td>
</tr>
</tbody>
</table>

NOTE
For LSB value for range and resolution used, see Table III.
*Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltage Range and LSB Values

<table>
<thead>
<tr>
<th>Analog Input Voltage Range</th>
<th>±10 V</th>
<th>±5 V</th>
<th>±2.5 V</th>
<th>0 V to +10 V</th>
<th>0 V to +5 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>COB*</td>
<td>COB*</td>
<td>COB*</td>
<td>CSB***</td>
<td>CSB***</td>
</tr>
<tr>
<td>Designation</td>
<td>or CTC**</td>
<td>or CTC**</td>
<td>or CTC**</td>
<td></td>
<td></td>
</tr>
<tr>
<td>One Least FSR Significant</td>
<td>FSR</td>
<td>2^n</td>
<td>2^n</td>
<td>2^n</td>
<td>2^n</td>
</tr>
<tr>
<td>(Bit LSB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n = 8</td>
<td>78.13 mV</td>
<td>39.06 mV</td>
<td>19.53 mV</td>
<td>39.06 mV</td>
<td>19.53 mV</td>
</tr>
<tr>
<td>n = 10</td>
<td>19.53 mV</td>
<td>9.77 mV</td>
<td>4.88 mV</td>
<td>9.77 mV</td>
<td>4.88 mV</td>
</tr>
<tr>
<td>n = 12</td>
<td>4.88 mV</td>
<td>2.44 mV</td>
<td>1.22 mV</td>
<td>2.44 mV</td>
<td>1.22 mV</td>
</tr>
<tr>
<td>n = 14</td>
<td>2.44 mV</td>
<td>1.22 mV</td>
<td>0.61 mV</td>
<td>1.22 mV</td>
<td>0.61 mV</td>
</tr>
<tr>
<td>n = 15</td>
<td>1.22 mV</td>
<td>0.61 mV</td>
<td>0.31 mV</td>
<td>0.61 mV</td>
<td>0.31 mV</td>
</tr>
</tbody>
</table>

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement—achieved by using an inverter to complement the most significant bit to produce (MSB).
***CSB = Complementary Straight Binary.

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 2 and 3, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and –FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10 V Range: Set analog input to +1 LSB = 0.00061 V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR – 2 LSB = +9.99878 V. Adjust Gain for 00000000000001 digital output code; full scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000 V; digital output code should be 01111111111111.

−10 V to +10 V Range: Set analog input to −9.99878 V; adjust zero for 11111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756 V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000 V; digital output (complementary offset binary) code should be 01111111111111.
Figure 10. Analog and Power Connections for Bipolar 
-10 V to +10 V Input Range

Other Ranges: Representative digital coding for 0 V to +10 V and 
-10 V to +10 V ranges is given above. Coding relationships and 
calibration points for 0 V to +5 V, -2.5 V to +2.5 V and 
5 V to +5 V ranges can be found by halving proportionally the 
(corresponding code equivalents listed for the 0 V to +10 V and 
-10 V to +10 V ranges, respectively, as indicated in Table II.

Zero and full-scale calibration can be accomplished to a precision 
of approximately ±1/2 LSB using the static adjustment 
procedure described above. By summing a small sine or triangular 
wave voltage with the signal applied to the analog input, the 
output can be cycled through each of the calibration codes of 
interest to more accurately determine the center (or end points) 
of each discrete quantization level. A detailed description of this 
dynamic calibration technique is presented in Analog-Digital 
Conversion Handbook, edited by D. H. Sheingold, Prentice-Hall, 

GROUNDING, DECOUPLING AND LAYOUT
CONSIDERATIONS

Many data acquisition components have two or more ground 
pins which are not connected together within the device. These 
"grounds" are usually referred to as the Logic Power Return, 
Analog Common (Analog Power Return) and Analog Signal 
Ground. These grounds (Pins 8 and 30) must be tied together 
at one point for the AD1380 as close as possible to the 
converter. Ideally, a single, solid analog ground plane under 
the converter would be desirable. Current flows through the wires 
and etch stripes on the circuit cards, and since these paths have 
resistance and inductance, hundreds of millivolts can be generated 
between the system analog ground point and the ground 
pins of the AD1380. Separate wide conductor stripe ground 
returns should be provided for high resolution converters to 
minimize noise and IR losses from the current flow in the path 
from the converter to the system ground point. In this way 
AD1380 supply currents and other digital logic-gate return 
currents are not summed into the same return path as analog 
signals where they would cause measurement errors.

Each of the AD1380 supply terminals should be capacitively 
decoupled as close to the AD1380 as possible. A large value 
capacitor such as 1 μF in parallel with a 0.1 μF capacitor is 
usually sufficient. Analog supplies are to be bypassed to the 
Analog Power Return pin and the logic supply is bypassed to the 
Logic Power Return pin.

The metal cover is internally grounded with respect to the 
power supplies, grounds and electrical signals. Do not externally 
ground the cover.

APPLICATION

AD1380 Dynamic Performance

High performance sampling analog-to-digital converters like the 
AD1380 require dynamic characterization to assure they meet 
or exceed their desired performance parameters for signal 
processing applications. Key dynamic parameters include signal-to-
noise ratio (SNR) and total harmonic distortion (THD), which 
are characterized using Fast Fourier Transform (FFT) analysis 
techniques.

The results of that characterization are shown in Figure 11. In 
the test a 13.2 kHz sine wave is applied as the analog input (i_a) 
at a level of 10 dB below full scale; the AD1380 is operated at a 
word rate of 50 kHz (its maximum sampling frequency).

The results of a 1024-point FFT demonstrate the exceptional 
performance of the converter, particularly in terms of low noise 
and harmonic distortion.

In Figure 11, the vertical scale is based on a full-scale input 
referred as 0 dB. In this way, all (frequency) energy cells can 
be calculated with respect to full-scale rms inputs.

The resulting signal-to-noise ratio is 83.2 dB, which corresponds 
to a noise floor of −93.2 dB.

Total harmonic distortion is calculated by adding the RMS 
energy of the first four harmonics and equals −97.5 dB. Increasing 
the input signal amplitude to −0.4 dB of full scale, causes 
THD to increase to −80.6 dB as shown in Figure 12.
The ultimate noise floor can be seen with low level input signals of any frequency. In Figure 14 the noise floor is at −94 dB, as demonstrated with an input signal of 24 kHz at 39.8 dB.

At lower input frequencies, however, THD performance is improved. Figure 13 shows a full-scale (−0.3 dB) input signal at 1.41 kHz. THD is now −96.0 dB.

Figure 13

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

Figure 14.